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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/075,559	02/14/2002	Noyan Kinayman	TYCO-15	8410
7590	03/01/2004		EXAMINER	
DUANE MORRIS LLP			DINH, TUAN T	
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100 College Road West		ART UNIT	PAPER NUMBER	
Princeton, NJ 08540		2827		

DATE MAILED: 03/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)	
	10/075,559	KINAYMAN ET AL.	
	Examiner Tuan T Dinh	Art Unit 2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) Responsive to communication(s) filed on \_\_\_\_.
- 2a) This action is FINAL.                            2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) Claim(s) 1-28 is/are pending in the application.
- 4a) Of the above claim(s) 19-28 is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_ is/are allowed.
- 6) Claim(s) 1-18 is/are rejected.
- 7) Claim(s) \_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All    b) Some \* c) None of:
  1. Certified copies of the priority documents have been received.
  2. Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
 Paper No(s)/Mail Date 3.7
- 4) Interview Summary (PTO-413)  
 Paper No(s)/Mail Date. \_\_\_\_.
- 5) Notice of Informal Patent Application (PTO-152)
- 6) Other: \_\_\_\_.

## **DETAILED ACTION**

### ***Election/Restrictions***

1. Applicant's election of Group I (claims 1-18) in Paper No. 8 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

### ***Claim Objections***

2. Claims 4 and 14 are objected to because of the following informalities:

Claims 4 and 14, line 2, applicant should define the "PTFE" material.

Appropriate correction is required.

### ***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-3, 5-6, 8, 10-13, and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Newman (U. S. Patent 5,455,456).

As to claim 1, Newman discloses a package (500, column 7, line 17) for an integrated circuit (510, column 7, line 24) as shown in figure 5, comprising:

a plurality of layers printed wiring board (502, 504, 506), adhesive layers (528, 530, 532, 534), power and ground planes (522, 526), a solder ball layer (556) sealably connectable to each other to form a package (500) having a cavity (550, 552, 554, column 7, lines 40-41) sized and shaped to receive the integrated circuit (510),

each layer being formed of a respective material (see figure 5), each respective material being suitable for use as a printed circuit board substrate,

at least one of the plurality of layers being a substrate (504, column 7, lines 18-19) having contacts (516b, column 7, lines 27-28) that are connectable to electrical contacts of the integrated circuit by wire bonds (514b), and

a bottom one of the layers (506, column 7, line 19) having a plurality of ball attach pads (the PWB 506 having the solder ball layer 556 including ball pads (not shown) to carry solder balls (536)), electrically connected to the contacts of the substrate.

As to claims 2 and 3, Newman discloses the package (500) in figure 5 wherein one of the layers is a superstrate (502, column 7, line 18) formed of the same material and above the substrate (504), the superstrate having a sufficiently high dielectric constant to provide isolation between a plurality of signal traces (520) on the substrate (504).

As to claim 5, Newman discloses the plurality of layers in figure 5 including at least 5 layers.

As to claim 6, Newman discloses a top (metal lid, see column 2, line 25, element 546, column 7, lines 43-44) of the plurality of layers being sufficiently rigid to maintain planarity of the package.

As to claim 8, Newman discloses the bottom layer (506) being formed of a glass reinforced hydrocarbon/ceramic laminate (column 1, lines 37-39).

As to claim 10, Newman discloses the contacts (516b) of the substrate (504) are arranged to accommodate a flip-chip mounting of the integrated circuit, see figure 5.

As to claim 11, Newman discloses an integrated circuit package assembly (500) as shown in figure 5, comprising:

an integrated circuit (510); and

a plurality of layers (see explanation, claim 1) sealably connectable to each other to form a package having a cavity (550, 552, and 554) sized and shaped to receive the integrated circuit (510), each layer being formed of a respective material, each respective material being suitable for use as a printed circuit board substrate (see figure 5),

at least one of the plurality of layers being a substrate (504) having contacts (516b) that are connectable to electrical contacts of the integrated circuit (510), and

a bottom one of the layers (506) having a plurality of ball attach pads, electrically connected to the contacts of the substrate (see the explained in claim 1).

As to claims 12-13, Newman discloses one of the layers in figure 5 being a superstrate (502) formed of the same material and above the substrate (504), the

superstrate having a sufficiently high dielectric constant to provide isolation between a plurality of signal traces on the substrate.

As to claim 16, Newman discloses the bottom layer (506-figure 5) being formed of a glass reinforced hydrocarbon/ceramic laminate (column 1, lines 37-39).

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 4 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Newman (U. S. Patent 5,455,456) in view of Arthur et al. (U. S. Patent 4,849,284).

As to claims 4 and 14, Newman discloses all of the limitations of the claimed invention as explained above, except for the substrate and superstrate being formed of material comprising PTFE with a ceramic filler.

Arthur et al. shows a multiplayer board (16-figure 3) having a plurality of substrate material (18, 20, and 22), and each of substrates being comprised of the ceramic filled fluoropolymeric material (ceramic filler with PTFE), column 5, and lines 15-19.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ a PTFE with ceramic filler in the substrate and

superstrate of the package of Newman, as taught by Arthur et al. for the purpose of exhibiting improved electrical performance and thermal expansion.

7. Claims 7, 9, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Newman (U. S. Patent 5,455,456) in view of Sawai et al. (U. S. Patent 5,814,883).

Regarding claim 7 and 15, Newman discloses all of the limitations of the claimed invention, except for the top layer is formed of FR4 epoxy glass laminate.

Sawai et al. shows a semiconductor device in figure 1 having a lid (11) made of FR4 epoxy glass, see column 5, lines 15-20.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ a lid made of FR4 epoxy glass in the package of Newman, as taught by Sawai et al., for the purpose of achieving moisture absorption.

Regarding claim 9, Newman discloses in figure 5 a layer (528) formed below the substrate having an opening (552) sized and shaped to accommodate a chip carrier on which the integrated circuit is mounted.

Newman does not disclose the layer formed below the substrate made by glass reinforced hydrocarbon/ceramic laminate.

Sawai et al. shows the semiconductor device in figure 1 having a layer (200, see an attaching paper) formed below a substrate (100, see attached paper) made by glass reinforced hydrocarbon/ceramic laminate.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ a layer made of glass reinforced hydrocarbon/ceramic

laminate in the package of Newman, as taught by Sawai et al., for the purpose of reducing heat dissipation.

8. Claims 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Newman (U. S. Patent 5,455,456) in view of Degani et al. (U. S. Patent 5,473,512).

Newman discloses an IC package (500) in figure 5 comprising an IC chip (510), a plurality of layers, one formed as a substrate (504), and one formed as a bottom layer (506) having a plurality of ball attach pads, and some other claim elements as explained in claims 1 and 11. However, Newman does not disclose a printed circuit board having a circuit board substrate with circuit traces and a plurality of devices thereon, and the device including at least one IC package.

Degani et al. shows a printed circuit board or a motherboard (100, column 6, line 41, figure 1), the motherboard having a board substrate with circuit traces (101, 102, 103, column 6, line 38) having a plurality of devices (not shown), the devices including at least one IC package (see figure 1).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize a printed circuit board (or a motherboard) incorporated with the IC package of Newman, as taught by Degani et al., in order to form an electronic package.

As to claim 18, Newman does not disclose at least one of the plurality of layers being formed from the same material as the printed circuit board substrate.

Degani et al. shows a printed circuit board (PCB 200) of a package having the same material as the motherboard (100), see column 6, lines 40-44).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ a material of a PCB same as a material of a motherboard in the assembly of Newman, as taught by Degani et al. for the purpose of reducing cost, and facilitated manufacture.

### ***Conclusion***

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Lin et al. and Carapella et al. disclose related art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T Dinh whose telephone number is 571-272-1929. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
Tuan Dinh  
February 06, 2004.